A Fine-Grained Dynamic Partitioning Against Cache-Based Timing Attacks via Cache Locking

Nicolas Gaudin, Vianney Lapôtre, **Guy Gogniat**, Pascal Cotret

Workshop on Security for Custom Computing Machines (SCCM)
Tuesday September 2, 2025, Leiden, The Netherlands

Summary

- Context
- State of the art
- Fine-grained locking mechanism
- Implementation with an N-way set associative cache
- Implementation with a randomization-based skewed cache
- Conclusion

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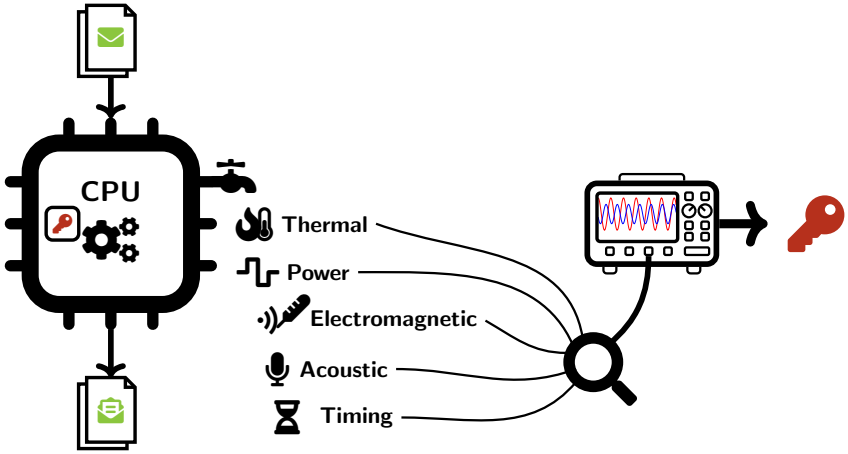
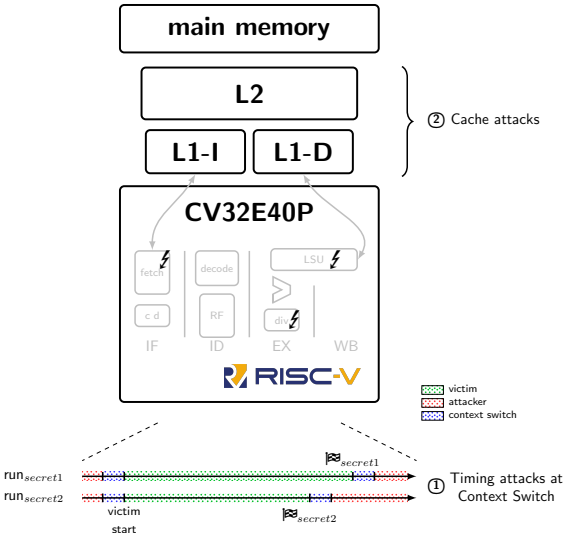
Side Channel Attacks (SCA)



Timing leakage



Sources of leakages exploited by :

Branching

if (condition(**secret**))

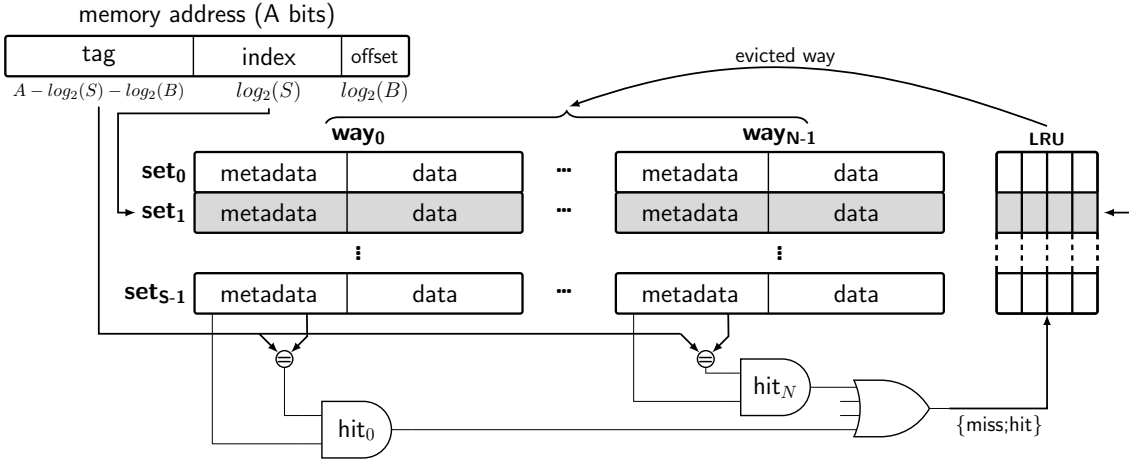
Operation with variable execution time

dividend/**secret**;

Index for Memory access

array[**secret**];

Cache Memories - N-way set associative cache



Prime+Probe attack

Objectives :

- Infer which cache set(s) is accessed by the victim
- Observe behavior of the attacker memory accesses

Requirements :

- Eviction Set matching with victim addresses
- Shared cache resource
- (High) Precision Timer

How ? :

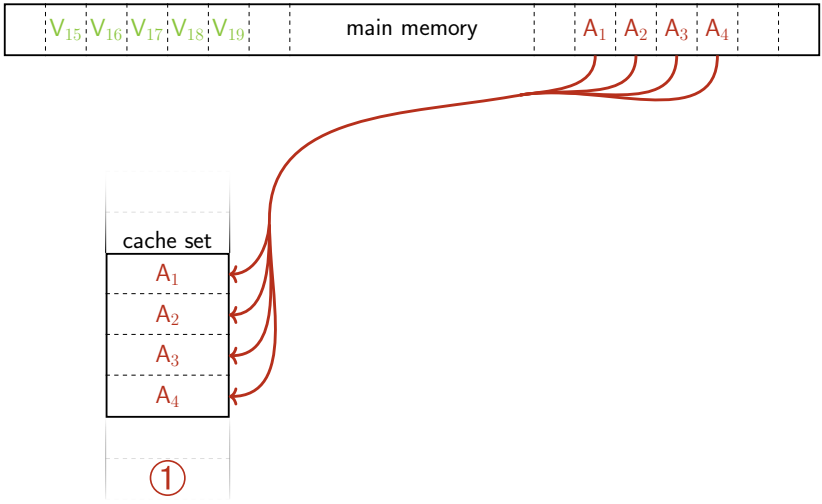
- with a 3-step attack

① fill a cache set using the eviction set

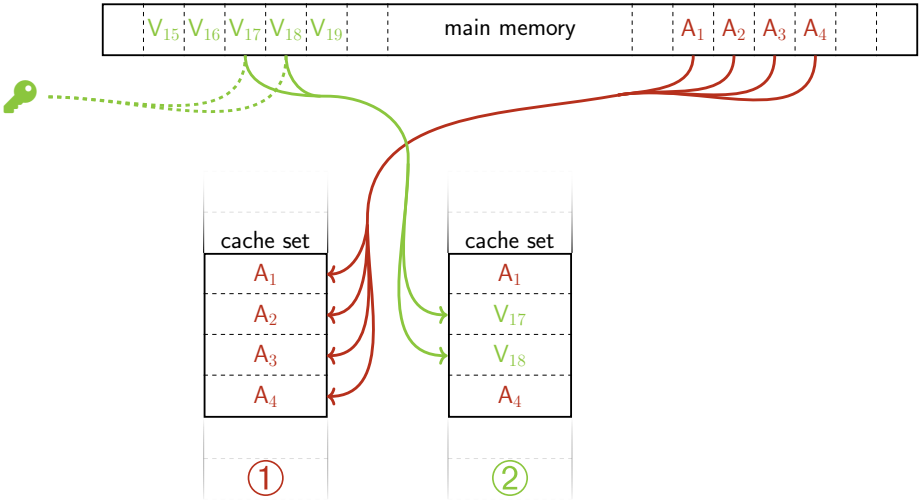
② let the victim execute

③ access and time each address of the eviction set

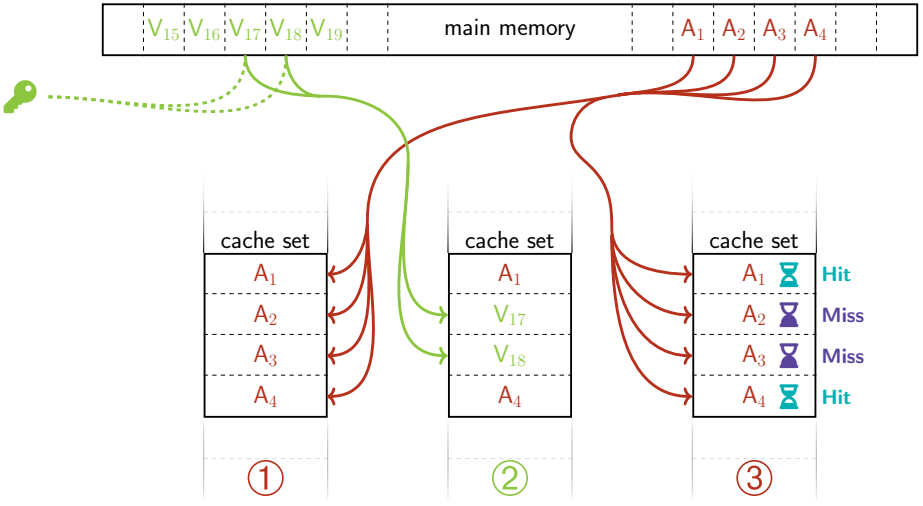
PRIME+PROBE attack



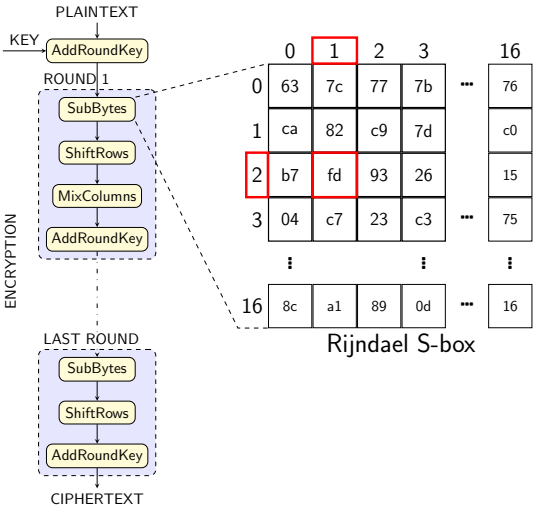
PRIME+PROBE attack



PRIME+PROBE attack

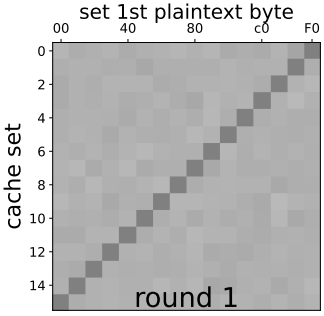


Considered attack on AES-128

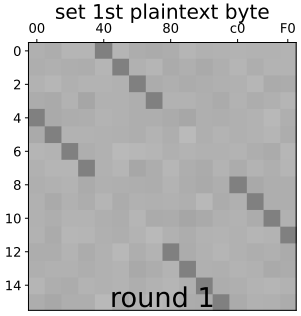


- SubBytes step accesses $\mathrm{SBOX}[P_i \oplus K_i]$
- Known plaintext attack

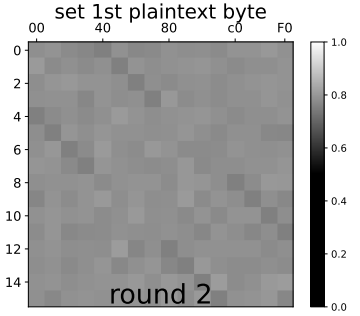
Example with PRIME+PROBE on AES-128



key = 0xFF



key = 0x42



key = 0x42

Summary

- Context
- State of the art
  - Randomization-based
  - Partitioning-based
- Fine-grained locking mechanism
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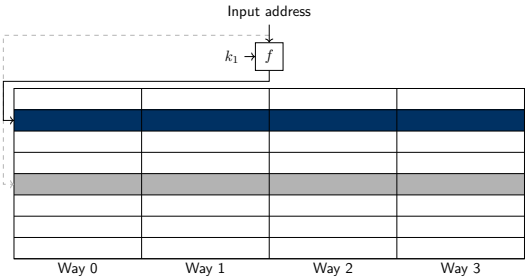
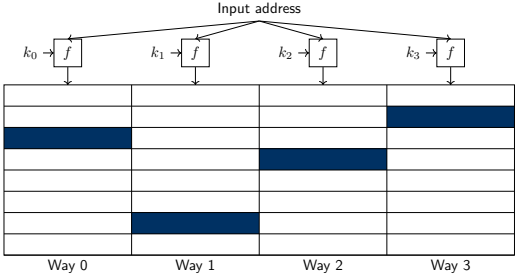
Randomization-based countermeasures - *Associative ways*



- Randomized the accessed cache set
  - Permutation table
  - Index Derivation Function

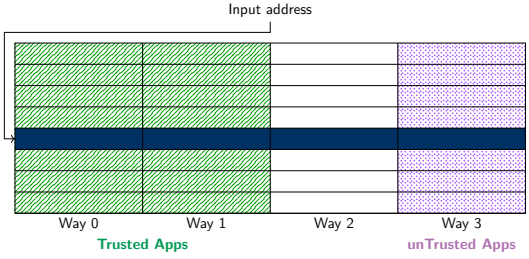
- RPcache [1]
- CEASER [2]
- ScrambleCache [3]
  - Easy to bypass this randomness [4]
  - Need to update primitives frequently
  - Maintain security costs performances

Randomization-based countermeasures - *Skewed ways*



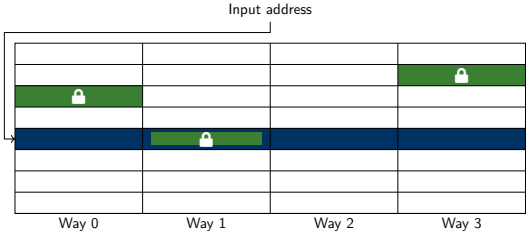
- Randomized accessed cache lines dissociating cache set
  - IDF for each way
- CEASER-S [5]
- ScatterCache [6]
  - Disruptive attack allows to find eviction set
  - PRIME+PRUNE+PROBE [4]
- ClepsydraCache [7]
  - Analog/digital costly design

Partitioning-based countermeasures - *coarse-grained*



- Partition resource to avoid conflicts
- Software-based :
  - COLORIS [8]
  - COTSknight [9]
- Hardware-based :
  - NoMoCache [10]
  - SecDCP [11]
    - Partitions do not meet needs

Partitioning-based countermeasures - *fine-grained*



- Partition resource to avoid conflicts
- Fine-grained :
  - Vantage [12]
  - PLcache [1]
    - Avoid conflict based attacks but leaks on LRU update

State of the Art Synthesis

- **Randomization-based**
  -  Autonomous
  -  Need to frequently update security (and so invalidate the cache)
- **Coarse Grained Partitionning**
  -  Provide a security support for OS/applications
  -  Can widely affect performances

---

- Countermeasures are designed considering complex system
  - Doesn't fit with embedded systems requirements/possibilities
  - Often focus on Last Level Cache (large shared cache)
- Not directly compatible with embedded systems

State of the Art Synthesis

- **Fine Grained Partitionning**
  - Provide a security support for OS/applications
  - Affect slightly performances

- PLcache is a candidate for our security mechanism
  - Introduce new instructions to reserve cache lines
  - Fit with embedded systems requirement and limitations

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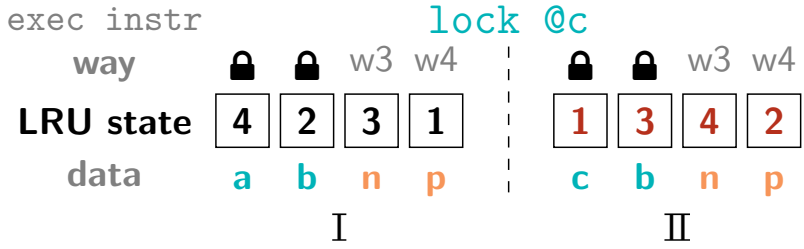
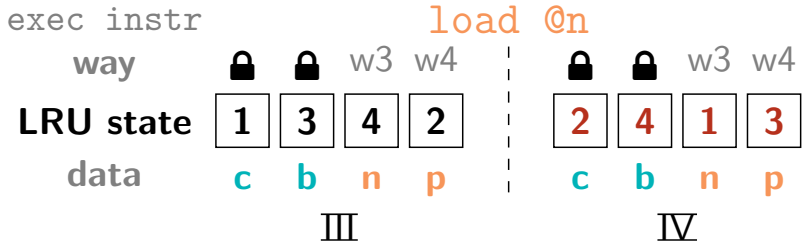
PLcache [1] issues



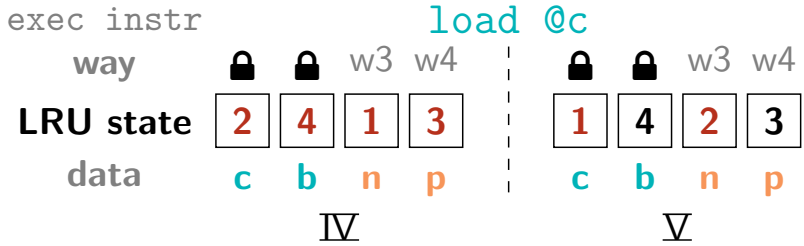
- No contant time accesses on locked data

PLcache [1] issues



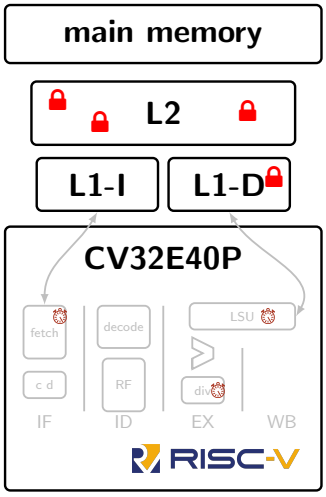
- No contant time accesses on locked data
- Shared LRU state among processes [13]

PLcache [1] issues



- No contant time accesses on locked data
- Shared LRU state among processes [13]

Our `lock` Mechanism

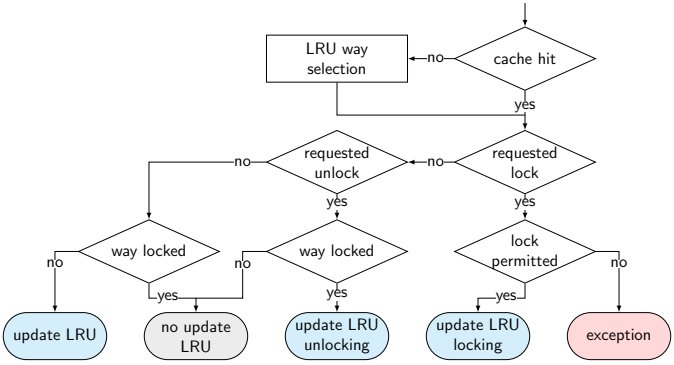


- Extend the Instruction Set Architecture
  - `lock` and `unlock` instructions

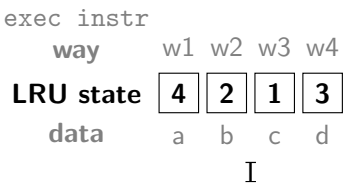
`lock` instr. keeps data cache line in cache
- guarantee constant time access
- locked cache line cannot be evicted
- mitigate EVICT+TIME and PRIME+PROBE

`unlock` instr. releases locked cache line
- data can be evicted

Cache access procedure with locking mechanism



Replacement policy update



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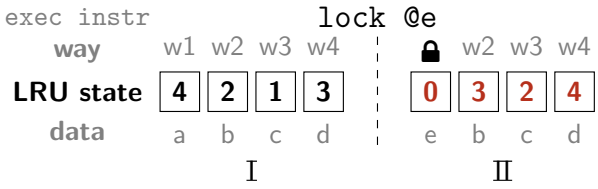
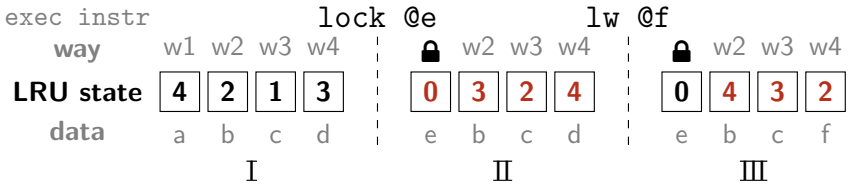


Replacement policy update



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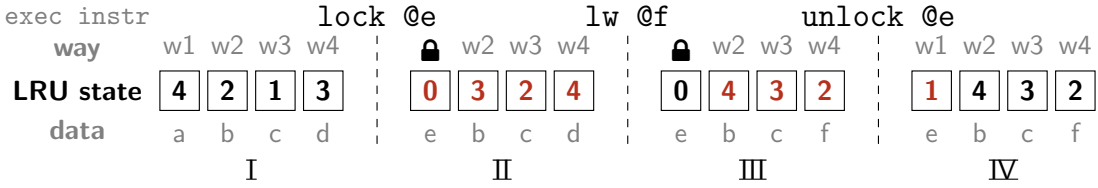

Software Implementation

```
1  void fct(int* sensitive_table, int* input){
2    //lock phase
3    for(int i=0; i<sizeof(sensitive_table); i+=16)
4      __LOCK(&sensitive_table, i);
5
6    //algo accessing table depending on secret
7    algo(sensitive_table, input);
8
9    //unlock phase
10   for(int i=0; i<sizeof(sensitive_table); i+=16)
11     __UNLOCK(&sensitive_table, i);
12 }
```

```
c.mv   t4,a4
c.mv   t5,a5
c.add  t4,t5
lock   x0,0(t4)
```

__LOCK macro

Listing 1: Example of use of the cache locking mechanism.

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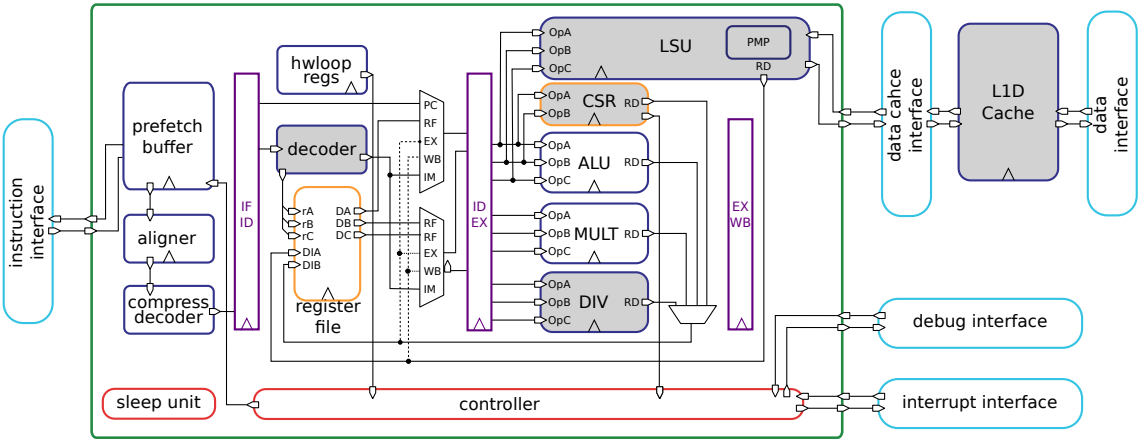
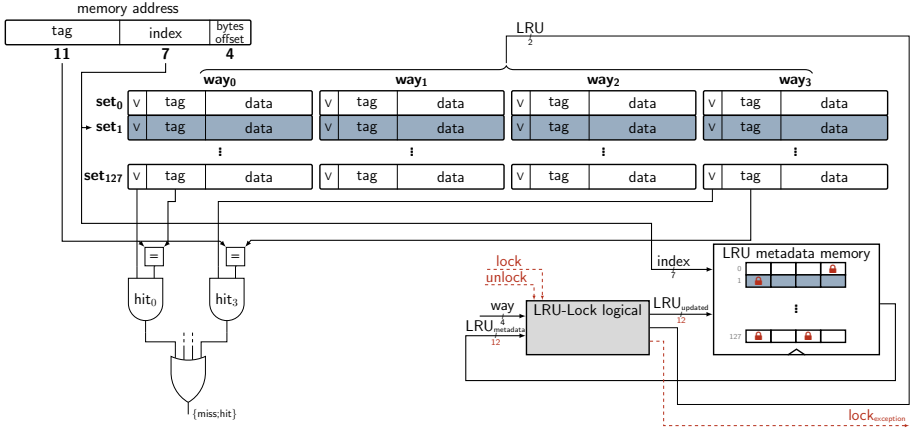
Implementation - *core level*

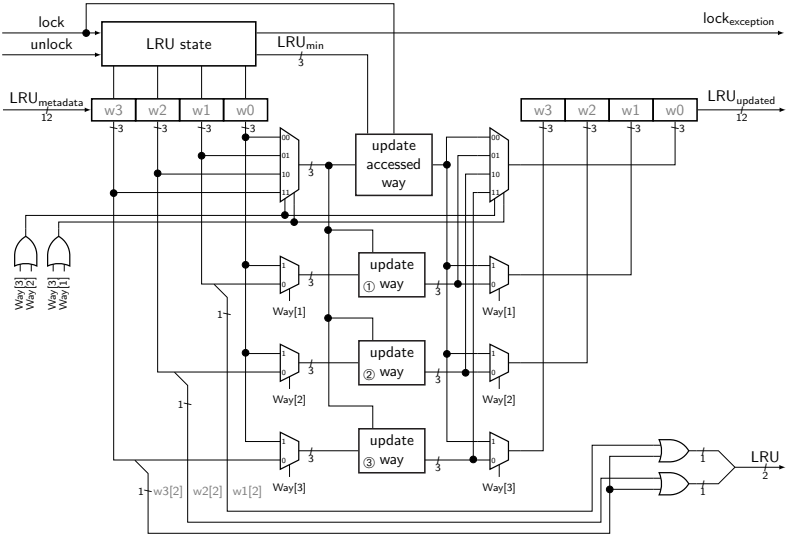


based on the OpenHWgroup CV32E40P core

Implementation - *cache level*



Implementation - *replacement policy level*



Impact on resource utilization

Post implementation area result

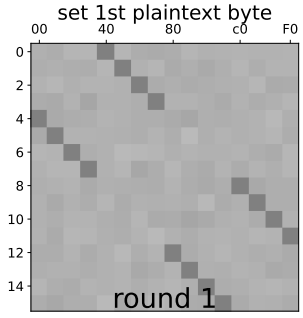
	without lock			with lock			Overhead	
	LUT	FF	BRAM	LUT	FF	BRAM	LUT	FF
↪ LRU	26	24	0,5	50	34	0,5	+ 92,31%	+ 41,67%
↪ Cache	980	1 065	8,5	1 007	1 077	8,5	**+ 2,76%**	**+ 1,1%**
↪ Core	4 669	2 233	0	4 666	2 235	0	- 0,06%	+ 0,09%
CPU	5 661	3 467	8,5	5 683	3 481	8,5	**+ 0,39%**	**+ 0,40%**

Considering AMD/Xilinx Kintex-7 FPGA family with Vivado 2022.2

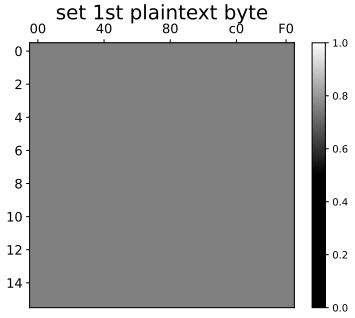
BRAM' Bits overhead

At cache level, baseline stores **72,704 bits** (cache lines + LRU metadata) + **512 bits** to implement our lock mechanism ▸ overhead of 0.7%.

Impact on Security - *considering* PRIME+PROBE *on AES-128*



Unprotected



using `lock`

Takeaway

The number of locked cache lines does not have to depend on secret.

Impact on Performances - *using `lock`*

Binary code size overhead

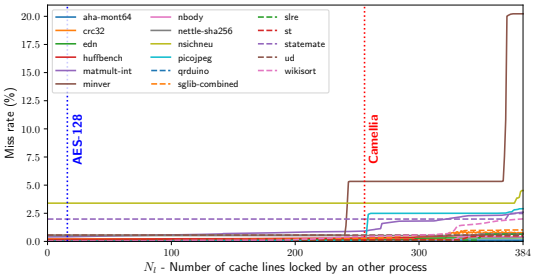
- AES-128 => **0,28%**
- Camellia => **0,23%**

Overhead induced by the insertion of `lock` and `unlock` instructions.

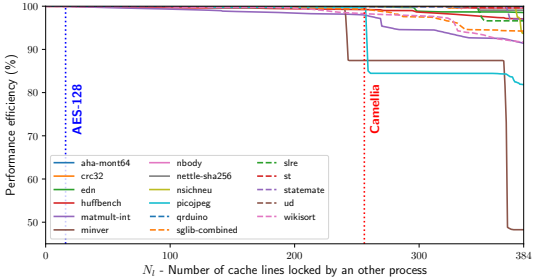
Execution time overhead (+%)

N_{Blocks}	1	4	8	16	64	128	512	1024
Camellia	367,7	99,6	54,22	28,88	7,62	3,85	0,97	0,48
AES-128	2,77	0,71	0,35	0,18	0,04	0,02	-	-

Impact on Performances - *on Embench-IoT benchmark*



Miss rate



Execution time

Takeaway

AES-128 and Camellia have a **negligeable impact** on Embench-IoT.

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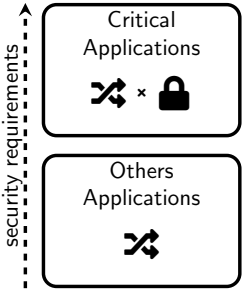
Goal of this implementation

- **Prevent** from a **new disruptive attack** to build eviction set (as PRIME+PRUNE+PROBE releases)
- Provide security guarantees while an eviction set is up
  - keep critical applications invulnerable
  - avoid attacker inferring number of locked cache lines
- Evaluate **hardware resource overhead** to implement such a system



🔀 maintains security for 6.8 M of memory accesses against P+P+P [14]

Post implementation area results

	skewed alone			**skewed with lock**			Overhead	
	LUT	FF	BRAM	LUT	FF	BRAM	LUT	FF
↦ VARP-64	88	85	2	135	138	2	+ 53,41%	+ 62,35%
↦ Data Cache	4 264	2 287	18	4 313	2 342	18	+ 1,15%	+ 2,30%
↦ VARP-64	100	85	2	99	85	2	- 1,0%	0,00%
↦ Instr Cache	3 214	2 178	18	3 212	2 178	18	- 0,06%	0,00%
↦ Key update	628	3 490	0	628	3 490	0	0,00%	0,00%
↦ Core	4 884	2 310	0	4 862	2 310	0	- 0,45%	0,00%
CPU	13 044	10 561	36	13 070	10 616	36	+ 0,20%	+ 0,52%

Considering AMD/Xilinx Kintex-7 FPGA family with Vivado 2022.2

Implementation Synthesis

At a glance :

- Provide **security guarantee** for critical applications
  - Skewed random cache for overall applications
  - Locking mechanism reserved for critical applications
- C**ritical applications remain immune** against known timing based CSCAs
- This implementation allows to defend against **new technique** to build eviction set
- Locking mechanism implementation implies a **low area** overhead (<2.5% on cache)

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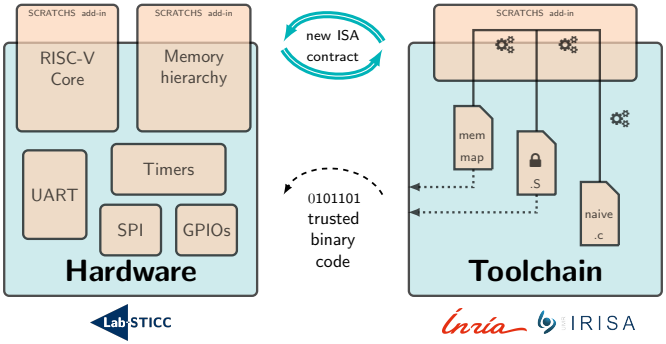
Conclusion

- We extend the RISC-V ISA to :
  - **guarantee cache hit** for memory accesses on locked data
  - mitigate Evict + Time, Prime+Probe
- The locking mechanism implementation implies a **low area** overhead (<3%)
- **Low** (negligeable) **impact** on overall performance
- The locking mechanism provides a **fine-grained** efficient and **on-demand security** against timing SCAs
- We demonstrate the light cost of locking in skewed implementation to harden security for critical application

SCRATCHS project

Side-**C**hannel **R**esistant **A**pplications **T**hrough **C**o-designed **H**ardware/**S**oftware



Ensure **efficient** and **on-demand** constant-time execution

List of publications in conferences

- N. Gaudin, J.-L. Hatchikian-Houdot, F. Besson, P. Cotret, G. Gogniat, G. Hiet, V. Lapotre, and P. Wilke, "Work in progress: Thwarting timing attacks in microcontrollers using fine-grained hardware protections," in *Proc. IEEE European Symposium on Security and Privacy Workshops (EuroS&PW)*, Jul. 2023. DOI: 10.1109/EuroSPW59978.2023.00038
- M. Peters, N. Gaudin, J. P. Thoma, V. Lapôtre, P. Cotret, G. Gogniat, and T. Güneysu, "On the effect of replacement policies on the security of randomized cache architectures," in *Proc. ACM Asia Conference on Computer and Communications Security (ASIA CCS)*, 2024, pp. 483–497. DOI: 10.1145/3634737.3637677
- N. Gaudin, P. Cotret, G. Gogniat, and V. Lapôtre, "A fine-grained dynamic partitioning against cache-based timing attacks via cache locking," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2024. DOI: 10.1109/ISVLSI61997.2024.00041

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